UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/916,197	07/27/2001	Chong Chin Hui	4712US (99-1054)	7070

24247 7590 02/04/2003

TRASK BRITT
P.O. BOX 2550
SALT LAKE CITY, UT 84110

EXAMINER
VIGUSHIN, JOHN B

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 02/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/916,197	Applicant(s) HUI ET AL.	
	Examiner John B. Vigushin	Art Unit 2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-79* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16,20-57,60-77 and 79* is/are rejected.

7)☒ Claim(s) *17-19,58,59 and 78* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 March 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *21 March 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The Examiner has reviewed the proposed changes to the drawings (filed as Paper No. 4 on March 21, 2002) and compared them to the concurrently submitted formal drawings (filed as Paper No. 5 on March 21, 2002) and notes that, in the amended Fig. 5, **the intended element number "42" and associated leader line have been inadvertently omitted in the formal version of Fig. 5**. Accordingly, a new formal drawing of Fig. 5 should be submitted which includes the missing element number "42" and associated leader line.

Rejections Based On Prior Art

2. The following references were relied upon for the rejections hereinbelow:

Takehara (US 6,476,507 B1)

Sasaki (US 6,175,159 B1)

Toh et al. (US 6,091,140)

Eng et al. (US 6,087,203)

Farnworth et al. (US 6,020,629)

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

4. Claims 21, 22, 26, 28, 33-41, 45-48, 51-57, 60-66, 70, 71, 73-77 and 79 are rejected under 35 U.S.C. 102(e) as being anticipated by Takehara.

As to Claim 21, Takehara discloses, in Figs. 1 and 6: a semiconductor die (1, 21) with at least one bond pad on an active surface thereof (col.7: 18-21); a tape (2, 29) secured to the active surface, the tape (2, 29) including a slot (corresponding to substrate openings 12, 22; col.7: 55-60; col.11: 43-45) formed therethrough with at least one bond pad being exposed through the slot (Figs. 1 and 6), at least one end of the slot extending beyond an outer periphery of the semiconductor die (1, 21) (col.11: 43-45); and a substrate element (3, 19) positioned over semiconductor die (1, 21) opposite the tape (2, 29) from the semiconductor die (1, 21), the substrate element (3, 19) including at least one opening (12, 22) formed therethrough through which the at least one bond pad is exposed (Figs. 1 and 6).

As to Claim 22, Takehara further discloses that the semiconductor die (1, 21) includes a plurality of bond pads is arranged substantially linearly along a central region of the active surface (Figs. 1 and 6).

As to Claim 26, Takehara further discloses that at least one end of the slot receives encapsulant material 7 (Figs. 2 and 3; col.8: 13-16: The at least one end of the

slot receives encapsulant material 7 when the encapsulant 7 is injected into the corresponding end of cavity 13 of coverlay 10).

As to Claim 28, Takehara further discloses substrate element (3, 19) comprises a carrier substrate for mounting semiconductor die (1, 21) and establishing electrical connection thereto and, in conjunction with solder bumps 6 for connection to an external circuit board, also functions as an interposer (Figs. 1 and 2).

As to Claim 33, Takehara further discloses that substrate element (3, 19) includes at least one contact area (receiving bond wire 4, 30) that corresponds to the at least one bond pad of semiconductor die (1, 21) (Figs. 1 and 6) and at least one contact pad 5 (Fig. 1) in electrical communication with the at least one contact area (col.7: 21-22).

As to Claim 34, Takehara further discloses that at least one intermediate conductive element--i.e., bonding wire (4, 30)--electrically connecting at least one die bond pad to the at least one contact area on the substrate element (3, 19).

As to Claim 35, Takehara further discloses at least one intermediate conductive element (4, 30) extends through the slot of tape (2, 29) and the at least one opening (12, 22) of substrate element (3, 19) (Figs. 1 and 6).

As to Claim 36, Takehara further discloses, in Figs. 2 and 3, a coverlay 10 disposed on a surface of substrate element 9 opposite another surface of the substrate element 9 positioned adjacent tape 2, the coverlay 10 positioned over the at least one opening 12 formed through substrate 9 (col.7: 54-60).

As to Claim 37, Takehara further discloses the coverlay 10 comprises a recessed area 13 configured to communicate with the at least one opening 12 (Figs. 2 and 3; col.7: 54-60).

As to Claim 38, Takehara further discloses that recessed area 13 is configured to receive a portion of at least one intermediate conductive element 4 electrically connecting the at least one bond pad of semiconductor die 1 to a contact area on a surface of substrate element 9 adjacent the at least one opening 12 formed therethrough (Figs. 2 and 3).

As to Claim 39, Takehara further discloses coverlay 10, at least one opening 12 formed through substrate element 9, the slot (corresponding to opening 12) formed through tape 2, and semiconductor die 1 together form a receptacle (Figs. 2 and 3).

As to Claim 40, Takehara further discloses, in Figs. 2 and 3, that the receptacle at least partially contains a quantity of encapsulant material (7, 8).

As to Claim 41, Takehara discloses, in Figs. 1 and 6: positioning a tape (2, 29) over the active surface of a semiconductor die (1, 21) so that the at least one bond pad on the at least one bond pad on the active surface is exposed through a slot (corresponding to opening 12, 22 in the substrate element 3, 19) formed through tape (2, 29) and at least one end of the slot extends beyond an outer periphery of semiconductor die (1, 21) (col.11: 43-45); positioning a substrate element (3, 19) over tape (2, 29) so that at least one bond pad is exposed through at least one opening (12, 22) formed through substrate element (3, 19) and aligned with the slot (col.11: 43-49), the substrate element (3, 19) including at least one contact area (to which at least one

bond wire 4, 30 is connected) corresponding to the at least one die bond pad (col.7: 18-21; col.11: 8-13); electrically connecting at least one bond pad to the at least one contact area (Fig. 1); positioning a coverlay 10 on an exposed surface of substrate element 9 (Figs. 2 and 3) to substantially cover the at least one opening (12, 22) formed through substrate element (3, 9, 19) (Figs. 1-3 and 6; col.7: 54-60); introducing encapsulant material 7 through at least one end into a receptacle formed by the coverlay 10, the at least one opening (12, 22), the slot, and the semiconductor die (1, 21) from a location opposite the semiconductor die (1, 21) from tape (2, 29) (Fig. 3; col.8: 13-19).

As to Claim 45, Takehara further discloses positioning tape (2, 29) comprises orienting the slot (which corresponds with opening 12, 22 in substrate 3, 19) with another end thereof extending laterally beyond the outer periphery of semiconductor die (1, 22) (col.11: 43-45).

As to Claims 46 and 47, Takehara further discloses securing, i.e., adhering tape (2, 29) to the active surface of semiconductor die (1, 21) (Fig. 2; col.7: 41-43).

As to Claim 48, Takehara discloses positioning substrate element 9 (a carrier substrate, which, in conjunction with solder bumps 6 for connection to an external circuit board, functions also an interposer) over tape 2 (Figs. 1 and 2).

As to Claims 51 and 52, Takehara further discloses connecting at least one intermediate conductive element (bonding wire 4, 30) between the at least one bond pad and the at least one contact area (Figs. 1 and 6).

As to Claim 53, Takehara further discloses extending the at least one intermediate conductive element (4, 30) through the slot formed through tape (2, 29) and the at least one opening (12, 22) formed through substrate element (3, 19) (Figs. 1 and 6).

As to Claim 54, Takehara further discloses positioning over substrate element (3, 9, 19) a coverlay 10 including a recessed area 13 alignable over at least one opening (12, 22) and over intermediate elements (4, 30) extending through at least one opening (12, 22) (Figs. 1-3 and 6; col.7: 55-60).

As to Claims 55 and 56, Takehara further discloses adhesively securing substrate element (3, 9, 19) to tape (2, 29) (Figs. 1 and 6; col.7: 16-18).

As to Claim 57, Takehara further discloses securing coverlay (10, 36) to substrate element 9 by means of plunger or vacuum induced pressure 37 (Figs. 3 and 7; col.10: 31-46; col.12: 15-25).

As to Claim 60, Takehara further discloses substantially filling the slot formed through tape (2, 29) and at least one opening (12, 22) formed through substrate element (3, 9, 19) with encapsulant material 7 (Figs. 1-3 and 6; col.8: 66-col.9: 1).

As to Claim 61, Takehara further discloses substantially encapsulating at least one intermediate conductive element (4, 30) electrically connecting the at least one die bond pad to the at least one substrate element contact area (Figs. 1-3 and 6).

As to Claim 62, Takehara further discloses positioning the coverlay 10 comprises forming the receptacle (Fig. 3), including the slot and the at least one opening, within which the at least one die bond pad is located (Figs. 2, 3 and 6).

As to Claim 63, Takehara discloses, in Figs. 1-3 and 6: positioning a tape (2, 29) over at least an active surface of a semiconductor die (1, 21), the tape (2, 29) including a slot (corresponding to substrate opening 12, 22) through which at least one bond pad on the active surface of the semiconductor die (1, 21) is exposed, at least a portion of the slot extending laterally beyond an outer periphery of semiconductor die (1, 21) (col.11: 43-45); positioning a substrate element (3, 9, 19) over tape (2, 29) with at least one opening (12, 22) formed through the substrate element (3, 9, 19) being located at least partially over the slot (Fig. 6); positioning a coverlay 10 over substrate element 9 to substantially seal the at least one opening 12, the coverlay 10 and lateral edges of at least one opening and the slot forming a receptacle (Figs. 2 and 3).

As to Claim 64, Takehara further discloses electrically connecting at least one die bond pad to at least one contact area located on a surface of substrate element (3, 9, 19) opposite tape (2, 29), proximate the at least one opening (12, 22) (Figs. 1 and 6; col.7: 18-20).

As to Claim 65, Takehara further discloses connecting at least one intermediate conductive element (4, 30) between at last one bond pad and the at least on contact area (Figs. 1 and 6; col.7: 18-20).

As to Claim 66, Takehara further discloses positioning the at least one intermediate conductive element at least partially within the slot and the at least one opening (12, 22) (Fig. 1).

As to Claims 70 and 71, Takehara further discloses adhesively securing tape (2, 29) to the active surface of semiconductor die (1, 21) (Fig. 2; col.7: 41-43).

As to Claim 73, Takehara discloses positioning substrate element 9 (a carrier substrate, which, in conjunction with solder bumps 6 for connection to an external circuit board, functions also as an interposer) over tape 2 (Figs. 1 and 2).

As to Claims 74 and 75, Takehara further discloses adhesively securing substrate element (3, 9, 19) to tape (2, 29) (Figs. 1 and 6; col.7: 16-18).

As to Claim 76, Takehara further discloses positioning over substrate element (3, 9, 19) a coverlay 10 including a recess 13 formed therein, the recess 13 positioned so as to communicate with the at least one opening (12, 22) formed through substrate element (3, 9, 19) when the positioning is effected (Figs. 1-3 and 6; col.7: 55-60).

As to Claim 77, Takehara further discloses securing coverlay (10, 36) to substrate element 9 by means of plunger or vacuum induced pressure 37 (Figs. 3 and 7; col.10: 31-46; col.12: 15-25).

As to Claim 79, Takehara further discloses removably securing the coverlay (10, 36) to substrate element (3, 9, 19) (col.9: 21-26).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2, 6, 7, 9, 10, 15, 16 and 20 are rejected under 35 U.S.C. 102(e) as anticipated by Takehara or, in the alternative, under 35 U.S.C. 103(a) as obvious over Takehara in view of Sasaki.

A) *As to Claim 1, rejected under 35 USC § 102(e) as anticipated by Takehara:*

Takehara discloses, in Figs. 1, 2 and 6: a semiconductor die (1, 21) with a plurality of bond pads arranged on an active surface thereof (col.7: 18-21); a tape (2, 29) positioned over the active surface, the tape 29 including at least one slot (corresponding to substrate openings 12, 22; col.7: 55-60; col.11: 43-45) formed therethrough, each of the plurality of bond pads being exposed through the at least one slot, at least one end of the at least one slot extending beyond an outer periphery of semiconductor die (1, 21) (col.11: 43-45); a substrate element (3, 19) positioned over tape (2, 29) opposite semiconductor die (1, 21), the substrate element (3, 19) including a plurality of contact areas, each contact area of the plurality corresponding to a bond pad of the plurality of bond pads and electrically connected thereto by way of an intermediate conductive element--i.e., bonding wire (4, 30)--that extends through at least one opening (12, 22; col.7: 55-60; col.11: 50-53) formed through the substrate element (3, 19) and aligned with the at least one slot of tape (2, 29) (Fig. 6; col.7: 18-21; col.11: 10-13 and 43-45), substrate element (3, 19) further including a contact pad 5 in communication with each contact area of the plurality of contact areas by way of a substantially laterally extending conductive trace in the substrate (col.7: 21-24) {*Examiner's Note: col.7: 21-22 recite "**[i]n** the substrate 3, **the wire** electrically connects **the pad** with an external terminal 5..." (bold emphasis by the Examiner). The*

*Examiner takes the position that "the wire" **in** the substrate is not referencing the bonding wire 4; rather "the wire" in, or a part of, the substrate is a **trace** (not shown), distinct from bonding wire 4. Furthermore "the pad" in the above-cited col.7: 21-22 is referring to "a pad (not shown) of the substrate 3" cited in col.7; 20-21 and **not** "a pad (not shown) of the semiconductor chip 1" cited in col.7: 19-20 because 'the wire"--i.e., trace-- in the substrate connects "the pad (not shown)" of the substrate to the terminal 5 of the substrate. Takehara does not provide any solid evidence of electrically connecting the contact bonding area of the substrate to the substrate terminal 5 with bonding wire 4 (e.g., none of the Drawings show such a construction and it is not entirely clear whether "the wire" in col.7: 19-20 is one and the same as bonding wire 4). Furthermore, the terminal 5 is configured to receive solder bump 6, and not configured to additionally receive a bonding wire 4. Therefore, the connection between the substrate terminal 5 and substrate wire-bond pad is evidently a "wire" **in** or **on** the circuit substrate 3; i.e., a trace}*; a quantity of encapsulant material (7, 28) substantially filling a volume defined by the at least one slot (corresponding to substrate openings 12, 22; col.11: 43-45) of tape (2, 29) and the at least one opening (12, 22) of the substrate element (3, 19).

B) *As to Claim 1, rejected under 35 USC § 103(a), as obvious over Takehara in view of Sasaki*:

I. Takehara discloses, in Figs. 1, 2 and 6: a semiconductor die (1, 21) with a plurality of bond pads arranged on an active surface thereof (col.7: 18-21); a tape (2, 29) positioned over the active surface, the tape 29 including at least one slot

(corresponding to substrate openings 12, 22; col.7: 55-60; col.11: 43-45) formed therethrough, each of the plurality of bond pads being exposed through the at least one slot, at least one end of the at least one slot extending beyond an outer periphery of semiconductor die (1, 21) (col.11: 43-45); a substrate element (3, 19) positioned over tape (2, 29) opposite semiconductor die (1, 21), the substrate element (3, 19) including a plurality of contact areas, each contact area of the plurality corresponding to a bond pad of the plurality of bond pads and electrically connected thereto by way of an intermediate conductive element--i.e., bonding wire (4, 30)--that extends through at least one opening (12, 22; col.7: 55-60; col.11: 50-53) formed through the substrate element (3, 19) and aligned with the at least one slot of tape (2, 29) (Fig. 6; col.7: 18-21; col.11: 10-13 and 43-45), substrate element (3, 19) further including a contact pad 5 in communication with each contact area of the plurality of contact areas by way of a "wire" (col.7: 21-24); i.e., "[i]n the substrate 3, the wire electrically connects the [substrate] pad with an external terminal 5, on which a solder bump 6....is provided" (col.7: 21-23).

II. Takehara does not discuss in the disclosure, or show in the drawings, how a "wire" such as bonding wire 4 is to be connected from the substrate wire-bonding contact area pad to the terminal pad 5 when the terminal pad 5 already has a solder bump 6 mounted thereon. Takehara also does not explicitly disclose a substantially laterally extending conductive trace connecting the substrate wire-bonding contact area to the solder-bumped terminal pad 5.

III. Sasaki discloses a carrier/interposer substrate 33 that mounts a semiconductor die 32 wherein bond wires 39 connect die 32 to wire-bonding pads 34a (i.e., contact areas) on substrate 33, and wire-bonding pads 34a are connected to external contact pads 34b (having solder balls 40 mounted thereon) by substantially laterally extending traces 34 (Figs. 1, 2A and 2B; col.5: 38-41 and 44-46).

IV. Since Takehara and Sasaki are in the same semiconductor packaging art and since Takehara refers to the wire "in the substrate 3" as "the wire" (Takehara, col.7: 21-22) and does not specifically and clearly identify it as one and the same as bonding wire 4 (bonding wire 4 clearly being an art-recognized bonding ***wire***), and since it is not likely or evidently practical that the bonding wire 4 would also be wire-bonded to an external contact pad 5 which already has a solder bump 6 attached thereto, then it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, in the carrier/interposer substrate of Takehara, the practical connection scheme between wire-bonding contact areas and external connection contact pads on the carrier/interposer substrate taught by Sasaki, wherein the wire-bonding contact areas are connected to solder-bumped external connection contact pads by means of substantially laterally extending **traces**. For even if Takehara actually contemplated the above-mentioned "wire" (see quote of the reference passage in section I, above) as a *bonding wire* (like bonding wire 4 in Fig. 1) for connecting the substrate wire-bonding contact area to the substrate solder-bumped external connection contact pad 5, such a "bonding wire" connection could easily become shorted with a neighboring bonding wire, which does not happen between traces printed/plated on, or in, the substrate, and

the traces of Sasaki can be better configured and dimensioned to both enable a higher density circuit layout on the substrate than can be achieved by bonding wires and avoid the parasitic induction effects common to looped bonding wire connections.

As to Claim 2, Takehara further discloses that the plurality of bond pads is arranged substantially linearly along a central region of the active surface of semiconductor die (1, 21) (Figs. 1 and 6).

As to Claim 6, Takehara further discloses that tape (2, 29) is adhesively secured to the active surface of semiconductor die (1, 21) and to substrate element (3, 19) (col.7: 16-18; col.11: 8-10).

As to Claim 7, Takehara further discloses substrate element (3, 19) comprises a carrier substrate for mounting semiconductor die (1, 21) and establishing electrical connection thereto, and, in conjunction with solder bumps 6 for connection to an external circuit board, functions also as an interposer (Figs. 1 and 2).

As to Claim 9, Takehara further discloses a quantity of encapsulant material (7, 28) substantially encapsulates each intermediate conductive element (4, 30) (Figs. 1 and 6).

As to Claim 10, Takehara further discloses a quantity of encapsulant material (7, 28) protrudes above a major plane of an exposed surface of substrate element (3, 19) opposite semiconductor die (1, 21) (Fig. 1).

As to Claim 15, Takehara further discloses a coverlay 10 positioned on a surface of substrate element 9 opposite tape 2, the coverlay 10 substantially covering at least

the at least one opening 12 through substrate element 9 (Figs. 2 and 3; col.7: 54-60; col.9: 46-50).

As to Claim 16, Takehara further discloses the coverlay 10 comprises a recessed area 13 within which each intermediate conductive element (4, 30) is contained (Fig. 3; col.7: 54-60; col.8: 8-13).

As to Claim 20, Takehara further discloses discrete conductive elements (bonding wires 4, 30) protruding from at least some of the contact pads (Fig. 1).

7. Claims 5, 25, 27 and 69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takehara (regarding Claims 5, 25, 27 and 69), or, in the alternative, Takehara in view of Sasaki (regarding Claim 5).

As to Claims 5, 25 and 69:

I. Takehara discloses all the limitations of each claim, and, in particular, discloses generally that the at least one slot formed through substrate opening (12, 22) and the corresponding slot in tape (2, 29) extends beyond an outer periphery of semiconductor die (1, 21) (col.11: 43-45). Takehara does not teach specific structural details of the "extends beyond an outer periphery..." limitation.

II. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the tape slot of Takehara such that two ends--i.e., both ends--of the tape slot extend beyond the outer periphery of the semiconductor die in order to meet the structural package requirements for a particular application and for facilitating an even distribution of resin flowed through the tape slot and corresponding substrate opening (12, 22).

As to Claim 27, Takehara further discloses that one of the two ends of the slot is positioned so as to facilitate displacement of air from the slot while a encapsulant material is being introduced at least into a volume defined by the slot from the other of the two ends (Figs. 2 and 3; col.8: 38-48: When the encapsulant 7 is injected into cavity 13 of the coverlay--disposed opposite the package slot--at one end of the package, the encapsulant then begins its flow at the corresponding end of the slot. As the injected encapsulant continues to flow along the slot, the air is displaced from the slot, escaping at the other end of the slot toward which the encapsulant flows).

8. Claims 8 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takehara (regarding Claims 8 and 44), or, in the alternative, Takehara in view of Sasaki

(regarding Claim 8), as applied to Claim 1 above, and further in view of Toh et al. and Farnworth et al.

As to Claims 8 and 44:

I. Takehara (or Takehara in view of Sasaki) discloses all the limitations of each claim but is silent as to the material of substrate element (3, 19) positioned over tape (2, 29).

II. Toh et al. discloses that silicon is old and well-known in the art as a material for a semiconductor die, being readily available and having certain practical electrical and mechanical properties suitable for a wide range of electronic components, packages and applications (col.5: 36-39 and 42-45).

III. Farnworth et al. discloses that it is beneficial to the structural integrity and performance reliability of a semiconductor package comprising a silicon die to also use silicon for the material of the carrier substrate in order to minimize thermal stress defects in the package such as warping and cracking which would adversely affect the performance of the semiconductor package (col.3: 34-40).

IV. Since Takehara as well as Toh et al. and Farnworth et al. are all in the same semiconductor electronics packaging art, then using a silicon die for the various semiconductor device applications taught by Toh et al. ***in conjunction with a silicon substrate*** having a coefficient of thermal expansion (CTE) that matches that of the silicon die, as taught by Farnworth et al., in order to avoid the problem of package warping and cracking during manufacture and operation, would have been readily recognized in the pertinent art of Takehara.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor die and substrate of

Takehara such that both comprise silicon in order to make use of the wide range of applications for a silicon die, as taught by Toh et al., and to provide a CTE match between the silicon die and the silicon substrate, as taught by Farnworth et al. for preventing package damage due to thermal stress forces during manufacture and operation, thereby ensuring the performance reliability of the semiconductor package.

9. Claims 3, 4, 11-14, 23, 24, 29-32, 42, 43, 49, 50, 67, 68 and 72 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takehara in view of Eng et al. (regarding Claims 3, 4, 11-14, 23, 24, 29-32, 42, 43, 49, 50, 67, 68 and 72), or, in the alternative, Takehara in view of Sasaki, as applied to Claim 1, above, and further in view of Eng et al. (regarding Claims 3, 4 and 11-14).

As to Claims 3, 42 and 67:

I. Takehara discloses all the limitations of each claim including tape (2, 29) positioned over the semiconductor die (1, 21) but is silent as to the relationship between the coefficients of thermal expansion of the adhesive tape material (2, 29) and the semiconductor die material (1, 21).

II. Eng et al. discloses that the adhesive layer 60 that connects the semiconductor die material 50 to substrate 70 is selected to have the same or similar coefficient of thermal expansion as that of the other components of the package 30--i.e., *die 50* and substrate 70--in order to minimize package damage and poor performance due to warping and cracking caused by thermal stress forces during manufacture (col.2: 6-18; col.7: 60-64; col.8: 51-52).

III. Since Takehara and Eng et al. are both in the art of semiconductor packaging wherein an adhesive layer or tape attaches a semiconductor die to a substrate, and the die is wire-bonded to the substrate for electrical connection, then the problem of overcoming package warpage and cracking during manufacture by matching the adhesive layer coefficient of thermal expansion (CTE) with the CTE of the other package components (i.e., *die 50* and substrate 70) would have been readily recognized in the pertinent art of Takehara.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the adhesive tape of Takehara by using a material with a CTE similar to or the same as the CTE of the die (as well as similar to or the same as the CTE of the other package components, such as the substrate), as

taught by Eng et al., in order to minimize thermal stress forces that would cause the package of Takehara to warp or crack, as taught by Eng et al., and thereby malfunction or perform unreliably.

As to Claims 4, 24, 43 and 68:

I. Takehara discloses all the limitations of each claim including the substrate element (3, 19) positioned over the tape (2, 29) but is silent as to the relationship between the coefficients of thermal expansion of the substrate element (3, 19) and the semiconductor die material (1, 21).

II. Eng et al. discloses that the adhesive layer 60 that connects the semiconductor die material 50 to substrate 70 is selected to have the same or similar coefficient of thermal expansion as that of the other components of the package 30--i.e., die 50 and substrate 70--and further teaches that the coefficient of thermal expansion of the substrate 70 should be considered in selecting the substrate material (col.3: 35-39 and 61-67), in order to minimize package damage and poor performance due to warping and cracking caused by thermal stress forces during manufacture (col.2: 6-18; col.7: 60-64; col.8: 51-52).

III. Since Takehara and Eng et al. are both in the art of semiconductor packaging wherein an adhesive layer or tape attaches a semiconductor die to a substrate, and the die is wire-bonded to the substrate for electrical connection, then the problem of overcoming package warpage and cracking during manufacture by matching the adhesive layer coefficient of thermal expansion (CTE) with the CTE of the other package components (i.e., die 50 and substrate 70), and, as strongly suggested in

col.7: 60-64 of Eng et al., by matching the CTE of the substrate 70 with the CTE of the material of die 50 (the "other components of integrated circuit package 30"), would have been readily recognized in the pertinent art of Takehara.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made modify the adhesive tape of Takehara by using a material with a CTE similar to or the same as the CTE of the die (as well as similar to or the same as the CTE of the other package components, such as the substrate), as taught by Eng et al., and further to use a material for the substrate with a CTE similar to or the same as the CTE of the semiconductor die, as strongly suggested by Eng et al. (col.3: 35-39 and 61-67; col.7: 60-64), in order to minimize thermal stress forces that would cause the package of Takehara to warp or crack, as taught by Eng et al., and thereby malfunction or perform unreliably.

As to Claims 11, 29, 49 and 72:

I. Takehara discloses all the limitations of each claim and further discloses an encapsulant 7 in substrate opening (12, 22) and the corresponding tape slot in order to cover and protect the bonding wires 4 and the bonding pads on the active surface of die (1, 21). Takehara does not teach a recessed area adjacent the at least one opening (12, 22), or adjacent at least a portion of an edge of the at least one opening (12, 22), located opposite tape (2, 29), each contact area of the plurality of substrate contact areas being located within the recessed area.

II. Eng et al. discloses a substrate 70 with an opening 86 (Figs. 1 and 2) located opposite adhesive layer 60 and exposing the semiconductor die bonding pads 120, the

substrate including a recessed area 86 adjacent central opening (at substrate layer 76), and in particular, adjacent at least a portion of an edge of the central opening, each substrate contact area 110 of the plurality of substrate contact areas being located within the recessed area (Figs. 1 and 2) for the purpose of providing a package structure for including an encapsulant 90 that protects the bond wires 80, the die bonding pads 120 and the substrate contact area 110, wherein the encapsulant and the die 50 are contained within the structure of the package such that the entire package assembly (i.e., substrate contact area surfaces and non-active die surfaces) need not be encapsulated, thus enabling a low package profile and overall small package size in keeping with the desirability in the industry for package miniaturization (col.8: 57-65; col.9: 13-16).

III. Since Takehara and Eng et al. are both in the semiconductor packaging art wherein the die, bond wires and die bonding pads to be protected, and Takehara includes package encapsulant that covers the entire die and portions of the circuitized substrate surfaces which adds to the profile of the package, then the recessed substrate structure taught by Eng et al. that requires encapsulant only within the recessed portion to cover and protect the bonding wires, die bonding pads and substrate contact area surfaces, all of which are *within* the recessed portion adjacent the central substrate opening, would have been readily recognized as in the pertinent art of Takehara for reducing the size of the semiconductor package in order to meet the consumer demand for miniaturization of electronic devices.

IV. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the substrate structure (3, 9, 19) in the package of Takehara by including in Takehara a recessed area adjacent the at least one opening (12, 22), and in particular, adjacent at least a portion of an edge of the at least one opening (12, 22), and located opposite adhesive tape (2, 29), each contact area of the plurality of substrate contact areas being located within the recessed area, as taught in the above-discussed substrate structure of Eng et al. (paragraph II, above), for the purpose of containing, at the very least, the protective encapsulant *within* the substrate, whereby no encapsulant is on the outer package surfaces, as taught by Eng et al., thus enabling a package having low profile and reduced size, as taught by Eng et al., in keeping with consumer demand for miniaturization of electronic devices.

As to Claims 12 and 50, Takehara, as modified by Eng et al. (see rejection of Claims 11 and 49, above), teaches that the quantity of encapsulant material substantially fills the recessed area (see Eng et al., Fig. 1, encapsulant 90 contained *within* the substrate 70 in recessed area 86 of the substrate 70), thus enabling a package having low profile and reduced size, as taught by Eng et al. (col.8: 57-65; col.9: 13-16), in keeping with the consumer demand for miniaturization of electronic devices.

As to Claim 13, Takehara, as modified by Eng et al. in Claims 11 and 12, above, teaches that the quantity of encapsulant material substantially encapsulates each intermediate conductive element, i.e., bonding wire in order to protect the bonding wires from the ambient environment (see Fig. 1 in Takehara; see Eng et al., Figs. 1 and 2, wherein encapsulant 90 substantially encapsulates each bonding wire 80).

As to Claim 14, Takehara, as modified by Eng et al., in Claims 11 and 12, above, teaches that the quantity of encapsulant material does not extend substantially beyond a major plane of an exposed surface of the substrate element (see Eng et al., Fig. 1, wherein encapsulant 90 is contained entirely within the substrate 70 in recessed area 86 and no encapsulant is on the outer package surfaces in order to enable a package having low profile, as taught by Eng et al. in col.8: 57-65 and col.9: 13-16).

As to Claim 23:

I. Takehara discloses all the limitations of base Claim 21 but is silent as to the relationship between the coefficients of thermal expansion of the adhesive tape material (2, 29) and the substrate element (3, 9, 19).

II. Eng et al. discloses that the adhesive layer 60, that connects the semiconductor die material 50 to substrate 70, is selected to have the same or similar coefficient of thermal expansion as that of the other components of the package 30--i.e., die 50 and *substrate 70*--and further teaches that the coefficient of thermal expansion of the substrate 70 should be considered in selecting the substrate material (col.3: 35-39 and 61-67), in order to minimize package damage and poor performance due to warping and cracking caused by thermal stress forces during manufacture (col.2: 6-18; col.7: 60-64; col.8: 51-52).

III. Since Takehara and Eng et al. are both in the art of semiconductor packaging wherein an adhesive layer or tape attaches a semiconductor die to a substrate, and the die is wire-bonded to the substrate for electrical connection, then the problem of overcoming package warpage and cracking during manufacture by matching the

adhesive layer coefficient of thermal expansion (CTE) with the CTE of the other package components (i.e., die 50 and *substrate 70*), would have been readily recognized in the pertinent art of Takehara.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made modify the adhesive tape of Takehara by using a material with a CTE similar to or the same as the CTE of the substrate element (as well as similar to or the same as the CTE of the other package components, such as the semiconductor die), as taught by Eng et al., in order to minimize thermal stress forces that would cause the package of Takehara to warp or crack, as taught by Eng et al., and thereby malfunction or perform unreliably.

As to Claims 30-32, Takehara as modified by the structure of Eng et al. (see rejection of Claim 29, above, and Figs. 1 and 2 in Eng et al.) further teaches that the modified substrate element 70 includes at least one contact area 110 corresponding to at least one bond pad 120 of die 50, the at least one contact area 110 is located within the recessed area 86, and the recessed area 86 receives a portion of an intermediate conductive element (bonding wire 80) that extends between the at least one bond pad 120 and the at least one contact area 110.

Allowable Subject Matter

10. Claims 17-19, 58, 59 and 78 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter:

As to Claims 17 and 18, patentability resides in the limitation wherein *the coverlay is secured to the substrate element with an adhesive material*, in combination with the other limitations of the broadest claim, Claim 17.

As to Claim 19, patentability resides in the limitation wherein *contact pads of the substrate element are exposed through or beyond the coverlay*, in combination with the other limitations of the claim.

As to Claims 58 and 59, patentability resides in *securing the coverlay to the substrate element with a pressure sensitive adhesive*, in combination with the other limitations of broadest claim, Claim 58.

As to Claim 78, patentability resides in *adhesively securing the coverlay to the substrate element*, in combination with the other limitations of the claim.

12. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Amagai (US 6,144,102) discloses at least one slot in an adhesive film 8 (which is the uppermost layer of tape-shaped substrate film 3) that exposes the bond

pads 2 of semiconductor die 1 (Figs. 1, 2 and 5; col.4: 18-27 and 60-61; col.5: 17-21; col.5: 64-col.6: 3; col.6: 14-16) but does not teach that the slot extends beyond an outer periphery of semiconductor die 1.

b) Huang et al. (US 6,218,731 B1) discloses that the adhesive material 122 which attaches the semiconductor die to substrate 104 may be a paste or a tape (Fig. 3; col.3: 60-63).

c) Jiang et al. (US 6,048,755) discloses that the adhesive material 72 which attaches the semiconductor die 16 to substrate 56 may be a filled or unfilled epoxy, an acrylic or a polyimide material (Fig. 7; col.6: 8-12).

d) Taguchi et al. (US 6,429,372 B1) discloses an optimal range of values of Young's Modulus (Modulus of Elasticity) for an adhesive layer 6 in the package of Figs. 2 and 3 subjected to a particular range of wire bonding temperatures during manufacture, the optimal range of Young's Modulus values resulting in an elasticity of the adhesive layer 6 that is sufficient to adequately support the film substrate 7 in order to achieve a wire bonding with suitable joint strength, as well as enable the absorption of thermal stress between the chip 1 and printed board 5 on which the package of Fig. 2 is mounted, as shown in Fig. 4 (col.2: 56-col.3: 6).

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

John B. Vigushin
Examiner
Art Unit 2827

jbv

January 31, 2003